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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,572	10/19/2001	Tom L. Nguyen	42390P12549	6116

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EXAMINER	
BESROUR, SAOUSSEN	

ART UNIT	PAPER NUMBER
2131	

MAIL DATE	DELIVERY MODE
06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/055,572	NGUYEN ET AL.	
	Examiner	Art Unit	
	Saoussen Besrour	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 3, 4 and 6-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 3, 4 and 6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to amendment filed 4/23/2007. Claims 1, 7, 10, 11, 12, 13, 14, 15, 16 17, 18 and 19 were amended. Claims 1, 2, 3, 4 and 6-19 are pending. Applicant's arguments/ amendments with respect to the claims have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Claim Objections

2. Corrections to the claims were received 4/23/2007, thus previous claim objections have been withdrawn.

Claim Rejections - 35 USC § 112

3. Previous 112, 2nd rejections have been withdrawn.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 2, 3, 4 and 6-19** are rejected under 35 U.S.C. 102(b) as being anticipated by Christenson (US 5,822,581).

As per **claim 1**, Christenson discloses: a first non-volatile data storage device, configured as one or more storage regions, to store one or more bytes of CMOS memory data, wherein the device lacks hardware security such that some of the CMOS memory data storage regions are modifiable by an application program on the system (Column 2, Lines 18-22, 38-50, Column 3, Lines 60-63, Column 4, Lines 29-35, 63-65); another, second non-volatile data storage device to store a mirror image of the CMOS memory data (Column 4, Lines 49-53, Column 5, Lines 4-5, 18-38); a program store to store one or more processor-readable instructions to ascertain the validity of the CMOS memory data stored in the first non-volatile storage device and when invalid to replace the CMOS memory data in the first non-volatile storage device with the stored mirror image of the data (Column 5, Lines 55-60); and a processing unit coupled to the first and second non-volatile data storage devices and program store, to read and process the one or more instructions in the program code (Fig. 1).

As per **claim 10**, Christenson discloses: reading CMOS memory content stored in a first non-volatile storage device of a system, wherein the first device lacks hardware security such that the CMOS memory content is modifiable by an application program in the system (Column 2, Lines 18-22, 38-50, Column 3, Lines 60-63, Column 4, Lines 29-35, 63-65); reading from a valid image of the CMOS memory content, that is stored in a further second non-volatile storage device (Column 4, Lines 49-53, Column 5, Lines 4-

5, 18-38); determining when the CMOS memory content in eth first device has been modified without authorization (Column 5, Lines 55-60); and replacing the CMOS memory content with said stored valid image when the CMOS memory content is determined to have been modified without authorization (Column 5, Lines 55-60).

As per **claim 17**, Christenson discloses: arranging a first non-volatile storage device of a computer system into one or more storage regions to store CMOS data (Column 2, Lines 18-22, 38-50, Column 3, Lines 60-63); generating an integrity metric corresponding to valid CMOS content stored in a first region of the first non-volatile storage device (Column 7, Lines 64-Column 8, Lines 25); and storing the integrity metric in another, second non-volatile storage device of the computer system to later determine if the content in the first region has been modified without authorization (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 2 and 16**, rejected as applied to claim 1 and 10. Furthermore, Christenson discloses: to process the instructions in the program store as part of a start-up procedure (Column 5, Lines 55-60).

As per **claim 3**, rejected as applied to claim 1. Furthermore, Christenson discloses: wherein the program store is inside the second non-volatile data storage device (Column 5, Lines 61-65).

As per **claim 4**, rejected as applied to claim 1. Furthermore, Christenson discloses: wherein the processor-readable instructions in the program store ascertain the validity of the data stored in the first non-volatile storage device on a region-by-region basis (Column 5, Lines 55-60 Fig. 3)

As per **claim 6**, rejected as applied to claim 4. Furthermore, Christenson discloses: employing a system interface to perform modifications to the data stored in said second non-volatile data storage device (Column 4, Lines 29-35 and Column 5, Lines 10-25).

As per **claim 7**, rejected as applied to claim 1. Furthermore, Christenson discloses: determining if current data in the first non-volatile storage device is different than the stored image of the data (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 8**, rejected as applied to claim 1. Furthermore, Christenson discloses: determining if an integrity metric corresponding to the current data in the first non-volatile storage device is different than the same integrity metric corresponding to the stored image of the data (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 9**, rejected as applied to claim 1. Furthermore, Christenson discloses: generating a copy of the current data in the first non-volatile memory device when an authorized application modifies the current data and storing the copy as a valid image of the current data (Column 4, Lines 29-35 and Column 5, Lines 10-25).

As per **claim 11**, rejected as applied to claim 10. Furthermore, Christenson discloses: comparing the valid image to the CMOS memory content to determine when the CMOS memory content has been modified (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 12**, rejected as applied to claim 10. Furthermore, Christenson discloses: comparing a previously stored checksum, corresponding to the valid image of

the CMOS memory content, and a checksum corresponding to the CMOS memory content (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 13**, rejected as applied to claim 10. Furthermore, Christenson discloses: comparing a previously stored cyclic redundancy check value, corresponding to the valid image of the CMOS memory content, and a cyclic redundancy check value corresponding to the CMOS memory content (Column 7, Lines 64-Column 8, Lines 25).

As per **claims 14**, rejected as applied to claim 10. Furthermore, Christenson discloses: comparing a previously stored bit mask, corresponding to the valid image of the CMOS memory content, and a bit mask corresponding to CMOS memory content (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 15**, rejected as applied to claim 10. Furthermore, Christenson discloses: storing a valid image of the CMOS memory content for later use (Column 8, Lines 1-25).

As per **claim 18**, rejected as applied to claim 17. Furthermore, Christenson discloses: comparing a previously stored integrity metric, corresponding to an earlier version of the content stored in the first region, to a newly calculated integrity metric corresponding to the current content stored in the first region to determine when an unauthorized modification has occurred (Column 7, Lines 64-Column 8, Lines 25).

As per **claim 19**, rejected as applied to claim 17. Furthermore, Christenson discloses replacing the content of the first region with an earlier version of the content therein when it is determined that there was unauthorized modification (Column 7, Lines 64-Column 8, Lines 25).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saoussen Besrour whose telephone number is 571-272-6547. The examiner can normally be reached on M-F 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SB
June 9, 2007

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